

April 1988 Revised September 2000

# 74F273 Octal D-Type Flip-Flop

#### **General Description**

The 74F273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ( $\overline{\text{MR}}$ ) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the  $\overline{MR}$  input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

#### **Features**

- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered, asynchronous Master Reset
- See 74F377 for clock enable version
- See 74F373 for transparent latch version
- See 74F374 for 3-STATE version

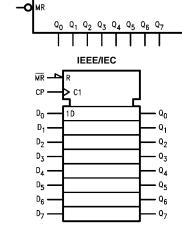
### **Ordering Code:**

Order Number	Package Number	Package Description
74F273SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F273PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0,300 Wide

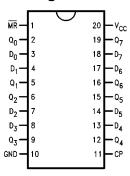
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

D<sub>3</sub> D<sub>4</sub> D<sub>5</sub> D<sub>6</sub> D<sub>7</sub>

#### **Logic Symbols**



### **Connection Diagram**



## **Unit Loading/Fan Out**

Pin Names	Promintion	U.L.	Input I <sub>IH</sub> /I <sub>IL</sub>	
Pin Names	Description	HIGH/LOW	Output I <sub>OH</sub> /I <sub>OL</sub>	
D <sub>0</sub> -D <sub>7</sub>	Data Inputs	1.0/1.0	20 μA/-0.6 mA	
MR	Master Reset (Active LOW)	1.0/1.0	20 μA/-0.6 mA	
СР	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/-0.6 mA	
Q <sub>0</sub> –Q <sub>7</sub>	Data Outputs	50/33.3	-1 mA/20 mA	

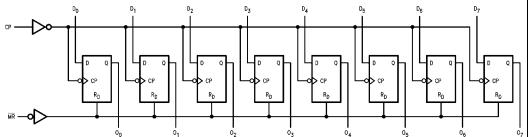
#### **Mode Select-Function Table**

		Output		
Operating Mode	MR	СР	D <sub>n</sub>	Q <sub>n</sub>
Reset (Clear)	L	Х	Х	L
Load "1"	Н	~	h	Н
Load "0"	Н	~	I	L

- H = HIGH Voltage Level steady state
  h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
  L = LOW Voltage Level steady state
- I = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
- X = Immaterial

  = LOW-to-HIGH clock transition

#### **Logic Diagram**



### **Absolute Maximum Ratings**(Note 1)

-65°C to +150°C Conditions

 $\begin{array}{ll} \mbox{Storage Temperature} & -65\mbox{°C to } +150\mbox{°C} \\ \mbox{Ambient Temperature under Bias} & -55\mbox{°C to } +125\mbox{°C} \\ \end{array}$ 

 $\begin{array}{lll} \mbox{Junction Temperature under Bias} & -55^{\circ}\mbox{C to } +150^{\circ}\mbox{C} \\ \mbox{V}_{\mbox{CC}} \mbox{ Pin Potential to Ground Pin} & -0.5\mbox{V to } +7.0\mbox{V} \end{array}$ 

 $\begin{array}{cc} \text{Input Voltage (Note 2)} & -0.5 \text{V to } +7.0 \text{V} \\ \text{Input Current (Note 2)} & -30 \text{ mA to } +5.0 \text{ mA} \end{array}$ 

Voltage Applied to Output in HIGH State (with  $V_{CC} = 0V$ )

 $\begin{array}{ll} \text{Standard Output} & -0.5 \text{V to V}_{\text{CC}} \\ \text{3-STATE Output} & -0.5 \text{V to +5.5 V} \end{array}$ 

Current Applied to Output

in LOW State (Max) twice the rated  $I_{OL}$  (mA) ESD Last Passing Voltage (min) 4000V

Free Air Ambient Temperature  $0^{\circ}\text{C} \text{ to } +70^{\circ}\text{C}$  Supply Voltage +4.5V to +5.5V

**Recommended Operating** 

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

#### **DC Electrical Characteristics**

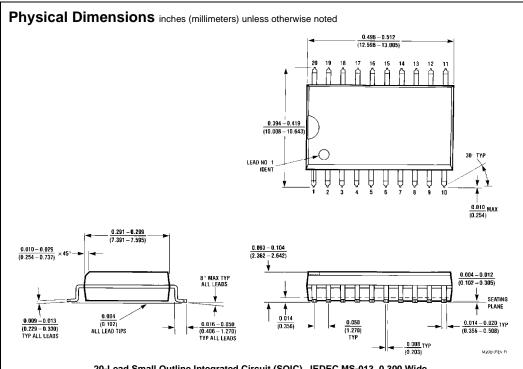
Symbol	Parameter		Min	Тур	Max	Units	v <sub>cc</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH	10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = -1 mA
	Voltage	$5\% V_{CC}$	2.7			V	IVIIII	IOH — — I IIIA
V <sub>OL</sub>	Output LOW	10% V <sub>CC</sub>			0.5	V	Min	1 - 20 mA
	Voltage	$5\% V_{CC}$			0.5	V	IVIIII	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH				5.0	μА	Max	V <sub>IN</sub> = 2.7V
	Current				3.0	μΛ	IVIAX	VIN - 2.7 V
I <sub>BVI</sub>	Input HIGH Current				7.0	μА	Max	V <sub>IN</sub> = 7.0V
	Breakdown Test				7.0	μΛ	IVIAX	VIN = 7.0V
I <sub>CEX</sub>	Output HIGH				50	μА	Max	V -V
	Leakage Current				50	μА	IVIAX	$V_{OUT} = V_{CC}$
V <sub>ID</sub>	Input Leakage		4.75			V	0.0	$I_{ID} = 1.9 \mu A$
	Test		4.73			V	0.0	All other pins grounded
I <sub>OD</sub>	Output Leakage				3.75	μА	0.0	V <sub>IOD</sub> = 150 mV
	Circuit Current				3.73	μΛ	0.0	All other pins grounded
I <sub>IL</sub>	Input LOW Current				-0.6	mA	Max	V <sub>IN</sub> = 0.5V
Ios	Output Short-Circuit Current		-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current				44	mA	Max	CP = _
I <sub>CCL</sub>					56	IIIA	IVIAX	$D_n = \overline{MR} = HIGH$

# **AC Electrical Characteristics**

Symbol	Parameter	$T_{A} = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_{L} = 50 \text{ pF}$		$T_{A} = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V$ $C_{L} = 50 \text{ pF}$		$T_A = 0$ °C to +70°C $V_{CC} = 5.0$ V $C_L = 50$ pF		Units	
		Min	Тур	Max	Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	160			95		130		MHz
t <sub>PLH</sub>	Propagation Delay	3.0		7.0	2.5	9.5	2.5	7.5	no
t <sub>PHL</sub>	Clock to Output	4.0		9.00	3.0	11.0	3.5	9.0	ns
t <sub>PLH</sub>	Propagation Delay	4.5		9.5	3.0	11.0	4.0	10.0	ns
t <sub>PHL</sub>	MR to Output			0.0	3.0	0	0	. 3.0	

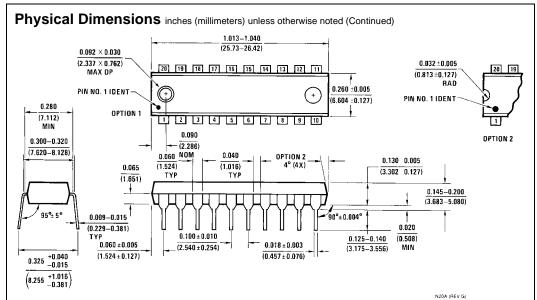
# **AC Operating Requirements**

Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$		$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = 5.0V$		$T_A = 0$ °C to +70°C $V_{CC} = 5.0V$		Units
		Min	Max	Min	Max	Min	Max	
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	3.0		3.5		3.0		
t <sub>S</sub> (L)	Data to CP	3.5		4.0		3.5		ns
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	0.5		1.0		0.5		
t <sub>H</sub> (L)	Data to CP	1.0		1.0		1.0		
t <sub>W</sub> (L)	MR Pulse Width, LOW	6.0		4.0		6.0		ns
t <sub>W</sub> (H)	CP Pulse Width	6.0		5.0		6.0		
$t_W(L)$	HIGH or LOW	6.0		5.0		6.0		ns
t <sub>REC</sub>	Recovery Time, MR to CP	3.0		4.5		3.5		ns



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M20B

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 2.6±0.10 0.40 TYP --A-5.01 TYP 5.3±0.10 9.27 TYP 7.8 -B-3.9 0.2 C B A ALL LEAD TIPS 10 PIN #1 IDENT.-- 0.6 TYP 1.27 TYP -LAND PATTERN RECOMMENDATION ALL LEAD TIPS SEE DETAIL A 0.1 C 2.1 MAX. 1.8±0.1 0.15±0.05 0.15-0.25 1.27 TYP 0.35-0.51 Ф 0.12 **М** C A > 7° TYP DIMENSIONS ARE IN MILLIMETERS GAGE PLANE 0.25 NOTES: A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998. B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. 0.60±0.15 SEATING PLANE 1.25 — M20DRevB1 DETAIL A 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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